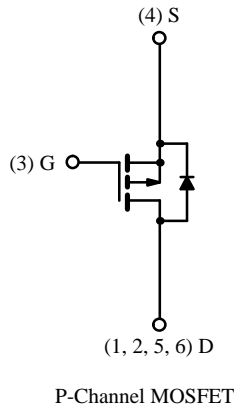
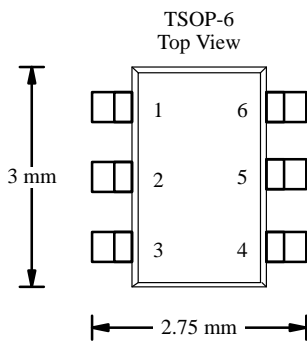


**P-Channel Enhancement-Mode MOSFET**

**Product Summary**

$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
-20	0.10 @ $V_{GS} = -4.5$ V	$\pm 3.3$
	0.135 @ $V_{GS} = -2.5$ V	$\pm 2.9$

**2.5-V Rated**



**Power Dissipation**  
**Si3441DV—2.0 W**

**Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$  Unless Otherwise Noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	$\pm 3.3$
		$T_A = 70^\circ\text{C}$	$\pm 2.6$
Pulsed Drain Current	$I_{DM}$	$\pm 20$	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	-1.6	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	2.0
		$T_A = 70^\circ\text{C}$	1.28
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

**Thermal Resistance Ratings**

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	62.5	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board,  $t \leq 5$  sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70191.

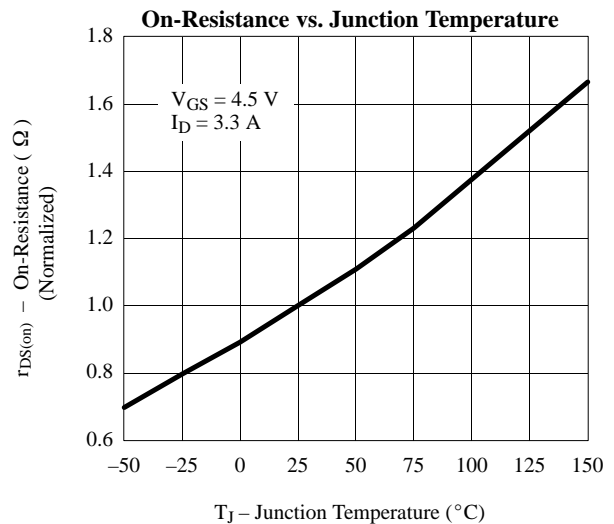
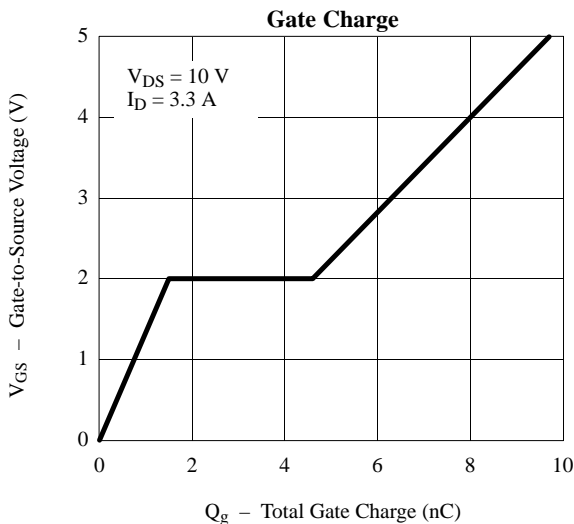
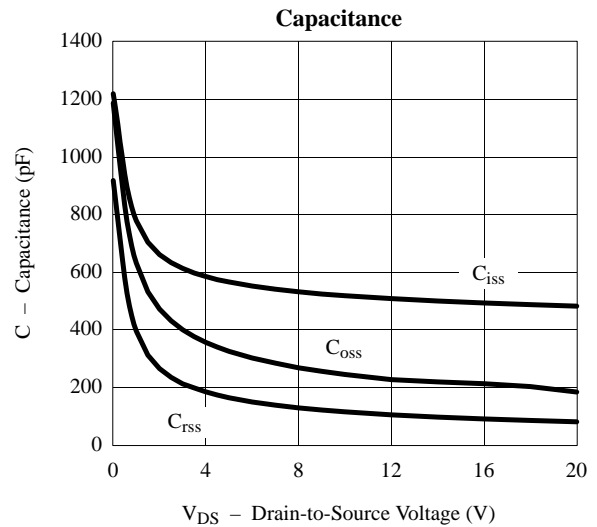
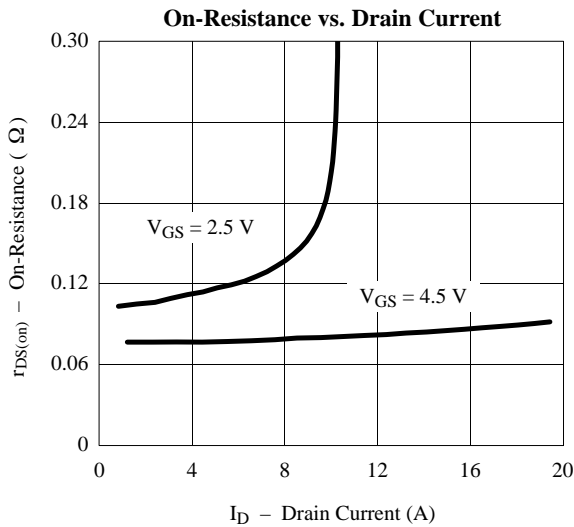
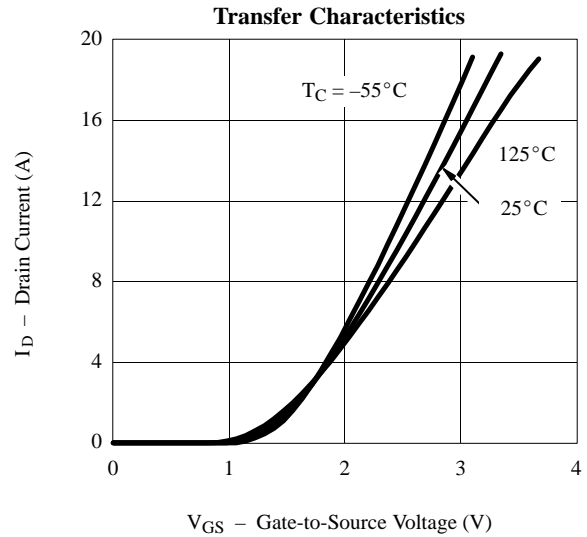
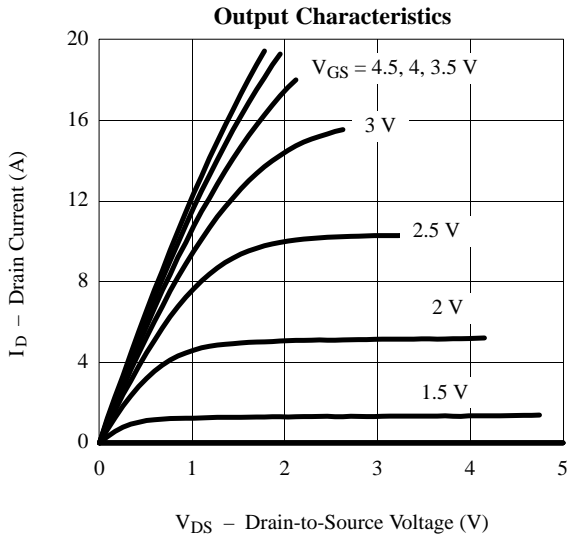
**Specifications ( $T_J = 25^\circ\text{C}$  Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	-0.45			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}$			-1	$\mu\text{A}$
		$V_{DS} = -20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-10			A
		$V_{DS} = -5\ \text{V}, V_{GS} = -2.5\ \text{V}$	-4			
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = 3.3\ \text{A}$		0.078	0.10	$\Omega$
		$V_{GS} = -2.5\ \text{V}, I_D = 2.9\ \text{A}$		0.110	0.135	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10\ \text{V}, I_D = -3.3\ \text{A}$		8.8		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = -1.6\ \text{A}, V_{GS} = 0\ \text{V}$		0.8	-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -3.3\ \text{A}$		8.6	14	nC
Gate-Source Charge	$Q_{gs}$			1.5		
Gate-Drain Charge	$Q_{gd}$			3.1		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong -1.6\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_G = 6\ \Omega$		27	50	ns
Rise Time	$t_r$			17	30	
Turn-Off Delay Time	$t_{d(off)}$			52	80	
Fall Time	$t_f$			45	70	
Source-Drain Reverse Recovery Time	$t_{rr}$		$I_F = -1.6\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	

## Notes

- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

**Typical Characteristics (25°C Unless Otherwise Noted)**



## Typical Characteristics (25°C Unless Otherwise Noted)

